

IN THE SPECIFICATION

Please insert the following paragraphs after line 2 of page 5:

By way of further background regarding methods of transmitting data, Figure 2 of U.S. Patent 4,977,577, previously incorporated by reference, shows a transmitter including chip-code-generation means, preamble means, address means, data means, timing means, pseudorandom-sequence means, and error-detection means. The chip-code-generation means may be embodied as a recirculating register 10 and the preamble means may be embodied as a preamble register 11. The chip-code-generation means may be embodied as a shift register with exclusive ORed feedback taps. The address means may be embodied as an address register 14, the data means may be embodied as a data register 18, and the error-detection means may be embodied as cyclical-redundancy-check (CRC) generator 19. The timing means may be embodied as timing circuit 13, and the pseudorandom sequence means may be embodied as the random number generator 17.

In the exemplary arrangement shown, a microprocessor 8 includes the recirculating register 10, preamble register 11, address register 14, data register 18, CRC generator 19, random number generator 17, and timing circuit 13. The timing circuit 13 is embodied as a timing algorithm in software, located in microprocessor 8. Alternatively, these registers and circuits may be put together with discrete components or independently wired and constructed as separate elements, as is well known in the art.

As shown in FIG. 8, an oscillator, which is shown as a voltage controlled oscillator 2 is coupled to an RF power amplifier 3, and the RF power amplifier 3 is coupled through a bandpass filter 4 to a micropatch or equivalent antenna 5. The voltage controlled oscillator 2 includes an enable input and a modulation input, where the voltage controlled oscillator generates a spread spectrum signal in response to a modulating voltage being applied to the

modulation input. The voltage controlled oscillator 2 is enabled by applying an enable signal to the enable input. The RF power amplifier 3 has a keying input and will amplify a signal from the voltage controlled oscillator 2 only if a keying signal is applied to the keying input. The voltage controlled oscillator 2 alternatively can be frequency locked to the microprocessor's crystal to improve stability. The voltage controlled oscillator 2 also can be replaced by a capacitor and inductor tuned oscillator and a phase shift keyed modulator, or any other means for generating a signal.

The microprocessor 8 is coupled to the modulation input of the voltage controlled oscillator 2 through first resistor R6 and second resistor R7. The microprocessor 8 broadly controls the voltage controlled oscillator 2 by supplying an enable signal to the enable input of the voltage controlled oscillator 2, and a modulating voltage to the modulation input of the voltage controlled oscillator 2. Also, the microprocessor 8 controls the RF power amplifier 3 by supplying a keying signal to the keying input of the RF power amplifier 3.

Included in the microprocessor 8 is a recirculating register 10 coupled to the modulation input of the voltage controlled oscillator 2 through second resistor R7. The recirculating register 10 stores a spread spectrum chip code, and outputs, during a transmitting interval, the spread spectrum chip code as a modulating voltage to the modulation input of voltage controlled oscillator 2.

The preamble register 11 is coupled to the modulation input of the voltage controlled oscillator 2 through first resistor R6. The preamble includes the coarse lock preamble and the fine lock preamble. The preamble register 11 stores a coarse lock preamble in cells 12 and a fine lock preamble in cells 24. The preamble register 11 outputs during the transmitting interval, the coarse lock preamble and the fine lock preamble as a modulating voltage to the modulation input of the voltage controlled oscillator 2 through first resistor R6. First resistor

R6 and second resistor R7 are chosen such that the desired spreading from the chip code and the data coming from the preamble register 11 is achieved.

Also shown in FIG. 8 is an address register 14 coupled to the modulation input of the voltage controlled oscillator 2 through the preamble register 11 and first resistor R6. The address register 14 stores a device address and a type code, and outputs during a transmitting interval, the device address and type code as a modulating voltage to the modulation input of the voltage controlled oscillator 2.

A data register 18 is coupled to a data input 20 and to the modulation input of the voltage controlled oscillator 2 through the preamble register 14 and the address register 11. The data register 18 stores data received from the data input, and outputs, during the transmitting interval, the data as a modulating voltage to the modulation input of the voltage controlled oscillator 2. The data from the preamble register 11, address register 14, and data register 18 are outputted in sequence, and at the end of a sequence, the cyclical redundancy check generator 19 outputs a data word at the end of the code for error detection.

A timing circuit 13 is included in microprocessor 8, and is coupled to the enable input of the voltage controlled oscillator 2 and to the keying input of the RF power amplifier 3 for enabling the voltage controlled oscillator 2 and the RF power amplifier 3, by outputting an enable signal to the enable input and a keying signal to the keying input of the RF power amplifier 3, respectively, during the transmitting interval. In essence, voltage controlled oscillator 2 and RF power amplifier 3 are not active or activated during a time duration of non-transmission, and are only activate during a transmission interval. The time duration between transmission intervals is made to vary in response to the random number generator 17 generating a random number and transferring the random number to the timing circuit 13. The random number modifies the timing duration between each transmitting interval randomly.

Also shown are the voltage supply, regulator circuit 1, and battery low detector 25.

The spread spectrum transmitter monitors one or more data inputs 20 and transmits periodically a supervisory data message. One or more of the data inputs 20 can be set 21 such that they cause a priority transmission at an increased rate higher than the supervisory message rate.

During installation of the transmitter, a device address (1-4095) 12, "Type" code 15 (fire, security, panic, heat, pull station, etc.) stored in preamble register 11, and a spread spectrum chip code stored in recirculating register 10 are loaded via programming connector 16. At installation time the "Panel" computer assigns the device ID address to each room number or unique device in the system which is to be monitored. The panel computer then prints a sticky label with the device's ID, address, type code and spread spectrum chip code, both in decimal and bar code form. The label is fixed to the smoke detector or alarming device and via the programming connector 16, or the number can be entered manually with the aid of a hand-held terminal. Alternatively a bar code reader can be connected to the programming connector 16 and the device can be read electronically from the bar code and entered into the transmitter. Microprocessor timing is controlled by crystal 23. Transmit timing is controlled by the wake-up timer 9, which has its own low power oscillator.

In operation, the transmitter sends a supervisory message often enough so that the receiver can detect failure of any transmitter within 200 seconds. The microprocessor 8 effectively "sleeps" between these transmissions to conserve battery life while counter 9 counts down to wake-up microprocessor 8. In order to minimize the chance of reoccurring data collisions from multiple simultaneous transmitters, the transmit interval is modified by random number generator 17. Very fine resolution intervals are used equal to 500 temporal transmit positions. The random number generator 17 is seeded with the transmitter's unique

address 14, resulting in different transmit schedules for each unit, thereby avoiding continuous collisions between transmitters.

Once the microprocessor 8 is reset by the wake-up circuit 9 the timing circuit 13 allows the crystal 23 to stabilize for 1-5 ms. The timing circuit 13 then enables the transmitter oscillator 2 and allows it to stabilize for 1 ms. The timing circuit 13 subsequently enables the RF amplifier 3 by sending a keying signal to the keying input. The RF energy from the RF amplifier 3 is filtered by bandpass filter 4 to reduce spurious RF emissions. The filtered signal is passed to a PCB foil micropatch 2 dBi gain antenna 5 which radiates the RF energy to an appropriate receiver. When the timing circuit 13 keys the RF power amplifier 3 it also begins to recirculate the spread spectrum 31 chip code stored in recirculating register 10 at a chip rate of 1 to 1.3 MHz. The chip code in turn causes a voltage swing 0-5 volts at the modulation input of the microprocessor. The voltage swing in conjunction with a modulation setting second resistor R7 creates a proportional current which modulates voltage controlled oscillator 2 thereby generating a spread spectrum FSK signal. This improves the signal to noise ratio at the receiver by reducing required bandwidth and minimizes the chances for intersecting interference. The data is super imposed on the chip code by the resistor 6 as a 1/31 deviation of the total modulation. Two or three adjacent chip code sequences are used to equal one bit time resulting in a baud rate of 14-21 KB/s.

In order for a receiver to demodulate a spread spectrum chip code, it must time lock onto the spread spectrum chip code. Disclosed are three methods of this timing acquisition, one is serial and two are parallel assisted. All methods require some synchronization bits in the transmitted message specifically allocated to code timing acquisition, which allow the receiver to search the code and find a correlation peak. The serial correlator searches one bit time per chip in the code sequence to achieve a plus or minus 1/2 chip code lock. This search can be hastened by searching one code sequence time instead of one bit time thereby

providing a two or three to one speed increase. The parallel correlator searches all 31 chip sequences in parallel so that an initial plus or minus $1/2$ chip synchronization ("lock") can be achieved in one bit or one chip code sequence time. "Fine" code lock ($\pm 1/4$ chip) for either serial or parallel assisted schemes must be followed by transmitted bit times allocated to allowing the receiver to achieve a higher resolution correlation "time" lock. One-quarter chip lock accuracies perform to within 1.25 dB of optimal code alignment. The receiver's fine code lock algorithm seeks to optimize the correlation peak. Higher levels of code lock can be achieved by searching in smaller fractions of a chip. This can facilitate "time of flight" distance or location measurement applications such that 25 ns, 25 feet, of measurement resolution can be achieved.

The transmitter's microprocessor 8 stores a synchronizing preamble in preamble register 11 of 36 bits for a serial correlator, which are broken into 31 bits for coarse lock 11 and 5 bits for fine lock 12. For the two parallel correlation methods disclosed 6 bits are used in the synchronizing preamble, 1 bit for coarse lock and 5 bits for fine lock. The actual code locking bits are transmitted as alternating ones and zeros so that the receiver's data demodulator can adaptively choose an optimal 1/0 voltage level decision point. The preamble is followed by a single data message synchronization bit 24 then 12 ID address bits 14 and 3 unit type bits 15 from address register 11, then 8 bits of input data from data register 18 and lastly 16 bits of CRC-16 data integrity check 19. The CRC-16 generator 19 is based on the entire proceeding message.

Once the message is transmitted, the timing circuit 13 turns off the enable signal at the enable input to voltage controlled oscillator 2 and the keying input of RF power amplifier 3, regenerates a new random number from random number generator 17, presets that number into the transmit interval wake-up circuit 9 and then sets the microprocessor 8 into the sleep

mode. Battery voltage regulation is provided by a micropower regulator 1. Battery voltage is pulse tested to conserve battery life 25.

The CRC-16 generator can have its kernel seeded with an identification number unique to each facility. For example, the kernel can be set by the facility address. Any facility having a transmission system which uses such a unique code as the kernel for the CRC-16 generator can be separated from adjacent facilities without additional transmission time or message bits.

Receiver

The spread spectrum receiver comprises several major blocks:

- A. The RF section which converts the received signal to lower frequencies;
- B. Chip code generator with means of chip code phase shifting for correlation lock;
- C. Means to measure both signal strength and quieting to detect correlation lock over the dynamic range of the system;
- D. An adaptive data demodulator tolerant to DC i.e.: long strings of 1's or 0's; and
- E. microprocessor algorithms to perform the above.

Please insert the following paragraph after line 21 on page 7:

Figure 8 is a transmitter described in U.S. Patent 4,977,577.

Please insert the following paragraph after line 20 on page 9:

Using the random generator shown in Figure 8, the time duration between transmission intervals in the present invention may be made to vary in response to the random number generator 17 generating a random number and transferring the random number to the timing circuit 13. The random number modifies the timing duration between each transmitting interval randomly.